Family list
4 application(s) for: **JP8080301 (A)**
Sorting criteria: Priority Date Inventor Applicant Ecla

1 **Transducer.**

Inventor: RESPAUT JAMES E [US]
EC: G10K11/35B2
Publication info: **DE3886170 (T2)** - 1994-04-14
Applicant: HEWLETT PACKARD CO [US]
IPC: ***A61B8/00; G01N29/04; G10K11/35;*** (+5)
Priority Date: 1987-10-30

2 **Transducer.**

Inventor: RESPAUT JAMES E
EC: G10K11/35B2
Publication info: **EP0314514 (A2)** - 1989-05-03
EP0314514 (A3) - 1989-11-15
EP0314514 (B1) - 1993-12-08
Applicant: HEWLETT PACKARD CO [US]
IPC: ***A61B8/00; G01N29/04; G10K11/35;*** (+5)
Priority Date: 1987-10-30

3 **CONVERTER SYSTEM**

Inventor: JIEIMUZU II RESUPOO
EC: G10K11/35B2
Publication info: **JP8080301 (A)** - 1996-03-26
Applicant: HEWLETT PACKARD CO
IPC: ***A61B8/00; G01N29/04; G10K11/35;*** (+5)
Priority Date: 1987-10-30

4 **Transducer with integral memory**

Inventor: RESPAUT JAMES E [US]
EC: G10K11/35B2
Publication info: **US4868476 (A)** - 1989-09-19
Applicant: HEWLETT PACKARD CO [US]
IPC: ***A61B8/00; G01N29/04; G10K11/35;*** (+4)
Priority Date: 1987-10-30

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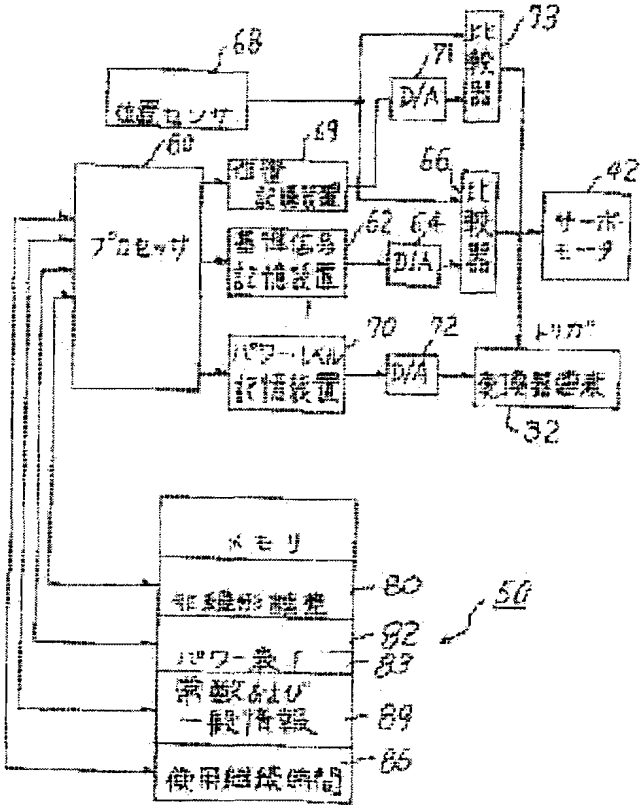
CONVERTER SYSTEM

Publication number: JP8080301 (A)
Publication date: 1996-03-26
Inventor(s): JIEIMUZU II RESUPOO +
Applicant(s): HEWLETT PACKARD CO +
Classification:
- international: ***A61B8/00; G01N29/04; G10K11/35;*** **A61B8/00; G01N29/04; G10K11/00;** (IPC1-7): A61B8/00; G01N29/04
- European: G10K11/35B2
Application number: JP19880274340 19881028
Priority number(s): US19870115689 19871030

Also published as:
EP0314514 (A2)
EP0314514 (A3)
EP0314514 (B1)
US4868476 (A)
DE3886170 (T2)

Abstract of **JP 8080301 (A)**

PURPOSE: To accurately position a converter element and to unify the scanning rate of the element by controlling the scanning of the converter element corresponding to the output of comparison means and correcting a reference signal for unifying the scanning rate on the basis of stored error correction information. CONSTITUTION: In a converter system, a processor 60 as compensation means for performing the compensation of error in the scanning of converter element 32 stores the error correction information in a memory device 50 which is mounted integrally to the converter element 32. Further, the processor 60 generates a reference signal of a servomotor 42 to control the converter element 32, and the position of the converter element detected by a position sensor 68 at a predetermined point of time is compared with the reference signal at a corresponding point of time by a comparator 66. Then, the processor 60 controls the scanning of the converter element 32 corresponding to the output of the comparator 66 with the servomotor 42, and correcting the reference signal for unifying the scanning rate on the basis of the error correction information stored in the memory device 50.



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(54)【発明の名称】　変換器システム

(57)【要約】
電子出願以前の出願であるので
要約・選択図及び出願人の識別番号は存在しない。